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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/966,222	09/28/2001	William James Palmteer	17658	5902

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EXAMINER	
ZARNEKE, DAVID A	
ART UNIT	**PAPER NUMBER**
2891	

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/966,222	PALMTEER ET AL.
	Examiner	Art Unit
	David A. Zarneke	2891

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *11 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-8 and 10-19* is/are pending in the application.

4a) Of the above claim(s) *10-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 4-8, 19* is/are rejected.

7)☒ Claim(s) *1* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

Claim 1 is objected to because of the following informalities: on line 10, the word "though" should be "through". Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, and 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori et al., US Patent 4,884,124.

Mori teaches a leadframe including (1) a die attach pad [7] centrally located thereon and (2) a plurality of wire bonding pads peripherally located therein (location where bond wires [4] attach to leadframe);

at least one aperture [7b, 7c, & 7d] formed fully through the die attach to separate the die attach onto different sections;

at least one die [1] having a first surface and an opposing second surface, the at least one die mounted on a section of the die attach pad such that substantially the entire opposing second surface is in mated contact with the die attach pad [figure 5], thereby forming a grounding path from said at least one die, through said section and to said circuit board;

at least one bonding wire [4] for electrically connecting the at least one die and at least one of the plurality of wire bonding pads; and

a mold compound [2], wherein said mold compound encapsulates the at least one die and the at least one bonding wire to form a chip scale package , and wherein the mold compound resides in the at least one aperture.

Regarding the limitation "suitable for use in a radio frequency (RF) range electronic device", it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations (Ex parte Masham, 2 USPQ2d 1647 (1987)).

While Mori fails to teach the leadframe is connected directly to a circuit board, it would have been obvious to one of ordinary skill in the art at the time of the invention to directly attach a leadframe to a circuit board because this is conventionally to which leadframes are bonded. The use of conventional materials to perform there known functions in a conventional process is obvious (MPEP 2144.07).

With respect to claim 4, while Mori fails to teach how the apertures are formed, the use of etching and half-etching to form the apertures is an obvious matter of design choice. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(I), (IVA) & (IVB)).

As to claim 5, Mori teaches the apertures to be in the shape of a rectangle or square (figure 6).

In re claim 6, Mori teaches a leadframe-based Chip Scale Package (figure 6).

Regarding claim 7, Mori teaches a plurality of apertures formed around the at least one die (figure 6).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mori et al., US Patent 4,884,124, as applied to claim 7 above, and further in view of Applicant's admitted prior art Figures 1A & 1B.

Mori fails to teach the use of a first and second die with apertures located between the two dice.

Applicant's admitted prior art teaches the use of a first and second die.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the first and second die of Applicant's admitted prior art in the invention of Mori because multiple dice on a leadframe saves money by using fewer materials, and also saves space by consolidating the dice onto one leadframe.

The apertures would inherently be located between the two dice because Mori teaches the die attach pad (7) as being covered with apertures outside the die attach area (figure 6).

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mori et al., US Patent 4,884,124.

Mori teaches a method for improving radio frequency grounding in a high dynamic range electronic device comprising operating a chip scale package at radio frequency (RF), said chip scale package comprising:

a leadframe including (1) a die attach pad [7] located thereon for connection directly to a circuit board and (2) a plurality of wire bonding pads peripherally located thereon (location where bond wires [4] attach to leadframe);

at least one aperture [7b, 7c & 7d] formed fully through the die attach to separate the die attach pad into different sections;

at least one die [1] having a first surface and an opposing second surface and being mounted on a section of the die attach pad such that substantially the entire opposing second surface is in mated contact with the die attach pad, thereby forming an RF grounding path from said at least one die, through said section, and into said circuit board (figure 6);

at least one bonding wire [4] for electrically connecting the at least one die and at least one of the plurality of wire bonding pads; and

a mold compound [2], wherein said mold compound encapsulates the at least one die and the at least one bonding wire to form a chip scale package, and wherein the mold compound resides in the at least one aperture (figure 6).

While Mori fails to teach the leadframe is connected directly to a circuit board, it would have been obvious to one of ordinary skill in the art at the time of the invention to directly attach a leadframe to a circuit board because this is conventionally to which leadframes are bonded. The use of conventional materials to perform there known functions in a conventional process is obvious (MPEP 2144.07).

Further, though Mori fails to teach operating a CSP at radio frequency, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a CSP operating at radio frequency because a CSP operated at radio frequency is conventionally kwon in the art, as evinced by applicant's own specification (page 2, lines

1+). The use of conventional materials to perform there known functions in a conventional process is obvious (MPEP 2144.07).

Conclusion

Any inquiry concerning this communication from the examiner should be directed to David A. Zarneke at (571)-272-1937. The examiner can normally be reached on M-Th 7:30 AM-6 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Baumeister can be reached on (571)-272-1712. The fax phone number where this application is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David A. Zarneke
Primary Examiner
May 27, 2005